ABSTRACT OF THE DISCLOSURE

A SONET multiplexed communications system that facilitates the sharing of processing resources while reducing overall system complexity. The SONET multiplexed communications system includes a single multi-output pointer generator clocked by a system clock and a plurality of clock domain transfer circuits having respective FIFO buffers for transferring SONET signals from the system clock domain to respective outgoing line clock domains. The multi-output pointer generator and the clock domain transfer circuits compensate for timing differences between the system clock and the respective outgoing line clocks by either skipping or overwriting FIFO buffer address locations corresponding to TOH byte positions in outgoing SONET frames. The TOH bytes corresponding to the skipped or overwritten TOH byte positions are subsequently re-generated by respective TOH insertion circuits before the outgoing SONET frames are passed through outgoing SONET lines.

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